

**RESPONSE TO NOTICE OF DRAWING INCONSISTENCY**

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Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

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**IN THE SPECIFICATION**

Please amend the paragraph beginning at page 9, line 4 as follows:

Figures ~~6A-6C~~ 6A-6D illustrate a number of address coincidence schemes that can be used together with the present invention.